REMARKS

Claims 1-3, 5-8, and 10-24 are pending in the application, of which claims 1, 6, 11, 16, and 22 are independent. Applicant has amended claims 1, 6, and 11 and reconsideration and re-examination are requested.

The Examiner rejected claims 1-3, 5-8, and 10-21 under 35 U.S.C. 103(a) as being unpatentable over Jain (US 6,044,211) in view of Bushard (US 5,819,072).

Claim 1 relates to a method of simulating a logic design. The method includes performing a three state simulation of the logic design to determine an output of the node in simulation... and determining if the three state simulation of the logic design was successful based on whether the output of the node has an undefined state, the three state simulation being successful if the output of the node is a defined state. The method also includes performing a four state simulation of the logic design if the three state simulation of the logic design was successful. Jain neither describes nor suggests claim 1 whether taken alone or in combination with Bushard.

The examiner states that Jain discloses performing a simulation of a logic design based on stored values of prior states and that Jain does not disclose four distinct state values. The examiner relies on Bushard to teach multi-state simulation using four logic states. While Bushard discloses a four state simulator (see FIG. 4 and col. 9, lines 31-37), Bushard fails to disclose performing the four state simulation if a three state simulation of the logic design was successful. In contrast, as shown in FIG. 7, Bushard performs a single, four state simulation.

In the examiner's response to arguments, the examiner states:

> Bushard teaches detecting (determining) if a simulation contains any unknown (i.e., undefined, not initialized) logic states and then storing the unknown states in a list (CL10, L9-11). Obviously, if no undefined states are determined during simulation, a four state simulation is simply not required since a four state simulation is only needed if undefined (i.e., fourth state) logic values exist... Hence, a skilled artisan that was aware of the teachings of Bushard (i.e. detecting the existence of undefined states), would have knowingly implemented the logic simulation design to perform a four state simulation only if undefined states actually exist... a three state simulation is all that is required if the circuit contains no undefined (i.e., unknown) values. (Office Action, pages 2-3).

Based on the examiner's comments, it appears that the examiner concedes that it would not have been obvious to perform a four state simulation if a three state simulation of the logic design was successful, that is, if the output of the node generated by the three state simulation is a defined state. Bushard fails to disclose or suggest performing a four state simulation after previously performing a three state simulation "if the three state simulation of the logic design was successful" as recited in claim 1. For all of the reasons acknowledged by the examiner, it would not be suggested to combine Jain and Bushard to perform a four state simulation if a three state simulation of the logic design was successful. For at least these reasons, applicant submits claim 1 should be allowed.

Claims 6 and 11 include similar limitations to claim 1 and are patentable for at least the reasons discussed in relation to claim 1. For at least the same reasons, applicant submits claims 1, 6, and 11 should be allowed, applicant submits that dependent claims 2-5, 7-10, and 12-15 should also be allowed.

Claim 16 includes "storing three bits of state information for a node included in a logic design, where the state information is represented by one of two possible values of the three bits of state information as a first bit of the three bits representing the presence or absence of a high state for the node, a second bit of the three bits representing the presence or absence of a logic

low state for the node, and a third bit of the three bits representing the presence or absence of an undefined state based for the node." Neither Jain nor Bushard disclose or suggest using a particular combination of the three bits to indicate the state of the node where each of the three bits represents the presence or absence of a particular condition. Thus, Jain whether taken alone or in combination with Bushard fails to disclose or suggest the method of the applicant's claim 16.

For at least the same reasons, applicant submits claim 16 should be allowed, applicant submits that dependent claims 17-21 are also allowable.

The Examiner rejected claims 22-25 under 35 U.S.C. 103(a) as being unpatentable over Chan (US 6,466,898) in view of Wang (6,738,875).

Claim 22 relates to a method for simulating a logic design using cycle based simulation. The examiner states that Chan does not explicitly disclose a write protected memory. In column 1, line 55 to column 2, line 7, as cited by the examiner, Wang teaches unprotecting a write protected page in response to a page fault such that the page can be accessed by the application. Wang fails to disclose or suggest "copying the instruction in a second memory page" and "executing the second memory page starting with the instruction" as recited in the applicant's claim 22.

For at least the same reasons, applicant submits claim 22 should be allowed, applicant submits that dependent claims 23-24 should also be allowed.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above

may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 2/8/06

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